CLAIMS

What is claimed is:

1. A method for performing a parallel hash transformation in a network device to generate a hash pointer for an address input, comprising:

receiving an address input;

apportioning the address input among a plurality of hashing units;

executing a hash transformation on the apportioned address inputs in parallel, resulting in a corresponding plurality of hashing unit outputs; and

combining the hashing unit outputs to generate a hash result corresponding to the address input.

2. The method of claim 1 wherein the address input is a 48-bit address input.

3. The method of claim 2 wherein the hash result is a 12-bit hash result.

4. The method of claim 1 wherein the address input is a 128-bit address input.

5. The method of claim 4 wherein the hash result is a 20-bit hash result.

6. The method of claim 1 wherein the hash transformations on the apportioned address inputs are configured to be executed in parallel within a single clock cycle such that the hash result is generated from the address input within the single clock cycle.

7. The method of claim 1 wherein the network device is a router configured to use the hash result for storing routing addresses with a routing table.

8. The method of claim 1 wherein the network device is a switch configured to use the hash result for storing forwarding addresses with a forwarding table.

9. A parallel hash transformation system for generating a hash pointer for an address input, comprising:

an input configured to accept an address;

a plurality of parallel hash units coupled to the input to receive respective portions of the address, the hashing units configured to execute a hash transformation on the respective portions of the address in parallel and generate respective hash outputs;

a combination unit coupled to receive the respective hash outputs, the combination unit configured to combine the respective hash outputs into a hash result; and

and output configured coupled to the combination unit to transmit the hash result.

10. The system of claim 9 wherein the input is configured to accept a 48-bit address input and the 48-bit address input is respectively apportioned among the parallel hash units.

11. The system of claim 10 wherein the hash result is a 12-bit hash result.

12. The system of claim 10 wherein the input is configured to accept a 128-bit address input and the 128-bit address input is respectively apportioned among the parallel hash units.

13. The system of claim 12 wherein the hash result is a 20-bit hash result.

14. The system of claim 9 wherein the hash transformations on the apportioned address inputs are configured to be executed in parallel within a single clock cycle such that the hash result is generated from the address input within the single clock cycle.

15. The system of claim 14 wherein the hash transformation system is implemented within a single hardware ASIC.

16. The system of claim 9 wherein the system is implemented within a router configured to use the hash result for storing routing addresses with a routing table.

17. The system of claim 9 wherein the system is implemented within a switch configured to use the hash result for storing routing addresses with a routing table.

18. The system of claim 9 further comprising:

a result storage register for storing the hash result coupled to the combination unit, the result storage register configured to transmit the hash result to the combination unit to enable a successive hash transformation on successive address inputs.

19. In a network device, a system for performing a parallel hash transformations, comprising:

means for receiving an address input;

means for dividing the address input among a plurality of hashing units;

means for executing a hash transformation on the apportioned address inputs in parallel, resulting in a corresponding plurality of hashing unit outputs; and

means for combining the hashing unit outputs to generate a hash result corresponding to the address input.

20. The system of claim 19 wherein the hash transformations on the divided address inputs are configured to be executed in parallel within a single clock cycle such that the hash result is generated from the address input within the single clock cycle.

21. The system of claim 19 wherein the network device is a router configured to use the hash result for storing routing addresses with a routing table.

22. The system of claim 19 wherein the network device is a switch configured to use the hash result for storing routing addresses with a routing table.

23. The system of claim 19 further comprising:

means for storing the hash result coupled to the combining means, the storing means configured to transmit the hash result to the combining means to enable a successive hash transformation on successive address inputs.

24. A computer readable media having stored thereon computer readable code for causing a network device to perform a method for parallel hash transformation to generate a hash pointer for an address input, the method comprising:

accessing an address input;

subdividing the address input into a plurality of portions;

performing a hash transformation on the portions in parallel, resulting in a corresponding plurality of hash portion outputs; and

reassembling the hash portion outputs to generate a hash result corresponding to the address input.

25. The media of claim 24 wherein the hash transformation on the portions of the address input are performed in parallel using a plurality of processors.